

ABSTRACT OF THE DISCLOSURE

A structure of a flash memory is provided. The flash memory has a charge trapping layer, a gate and a source/drain region, wherein the charge trapping layer is formed by stacking in sequence a first oxide layer, a dielectric layer of high dielectric
5 constant material and a second oxide layer. The gate is arranged on the charge trapping layer, and the source/drain region is arranged at the two lateral sides of the substrate.

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